

Low-Noise HEMT Using MOCVD

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Abstract—Low-noise HEMT AlGaAs/GaAs heterostructure devices have been developed using metal organic chemical vapor deposition (MOCVD).

The HEMT's with 0.5- μm -long and 200- μm -wide gates have shown a minimum noise figure of 0.83 dB with an associated gain of 12.5 dB at 12 GHz at room temperature. Measurements have confirmed calculations on the effect of the number of gate bonding pads on the noise figure for different gate widths. Substantial noise figure improvement was observed under low-temperature operation, especially compared to conventional GaAs MESFET's.

A two-stage amplifier designed for DBS reception using the HEMT in the first stage has displayed a noise figure under 2.0 dB from 11.7 to 12.2 GHz.

I. INTRODUCTION

TO MEET THE ever-increasing demands for low-noise, high-performance microwave circuits for satellite communications and other applications, development of very low noise devices for front-end amplifiers is being actively pursued in many laboratories [1], [2].

The limits of performance attainable using GaAs MESFET's are being approached by means of fine-pattern lithography and optimization of various device parameters. HEMT devices using AlGaAs/GaAs heterojunctions have displayed performance surpassing GaAs MESFET's within a short development period [3]. The heterojunction epitaxy for low-noise HEMT's has so far been performed using MBE (molecular beam epitaxy) by virtue of the high quality of the epitaxial interface.

We have previously reported on the microwave performance of our low-noise HEMT using MOCVD, or HIFET (hetero-interface FET), which has superior wafer throughput and surface quality (NF = 1.13 dB, PG = 10.8 dB at 12 GHz) [4].

In this paper, we will report on improvements made in the previous device performance by means of improvements in the epitaxy and device pattern and reduction of the gate length to 0.5 μm . A noise figure of 0.83 dB and an associated gain of 12.5 dB were measured at room temperature using 200- μm -wide devices.

II. DEVICE FABRICATION

The epitaxial layers necessary for the formation of the heterojunction structure are grown by MOCVD using tri-

methyl organometallics (TMA and TMG) and AsH₃ under atmospheric pressure. The growth temperature is 720°C and the growth rate is approximately 240 Å/min. The undoped GaAs layer is typically 5000 Å thick, while the initial thickness for the Si-doped n-AlGaAs layer is 690 Å at a doping level of $1.5 \times 10^{18} \text{ cm}^{-3}$. The net background impurity concentration of the undoped GaAs layer is under $2 \times 10^{15} \text{ cm}^{-3}$.

Hall mobilities of the two-dimensional electron gas created at the interface are 8030 and 148000 $\text{cm}^2/\text{V}\cdot\text{s}$ at 300 and 77 K, respectively, when using an undoped Al_{0.3}Ga_{0.7}As spacer layer of 100 Å.

The mobility and sheet carrier concentration of the two-dimensional electron gas (2DEG) are comparable to those reported using MBE.

A high mobility and a low sheet resistivity of the 2DEG are the most important parameters for realizing low-noise HEMT's. A high mobility of the 2DEG is desirable for low-noise operation, while a low sheet resistivity is required for reducing the source resistance.

A thin superlattice buffer (1000 to 2000 Å) of alternating undoped AlAs and GaAs layers and a 10-Å undoped AlGaAs spacer layer were introduced to satisfy the above requirements, as shown in the device cross section of Fig. 1. The 2DEG of the actual device showed a mobility of 5400 $\text{cm}^2/\text{V}\cdot\text{s}$ and a sheet resistivity of 800 Ω/square . When cooled to 77 K, the mobility increased to 26000 $\text{cm}^2/\text{V}\cdot\text{s}$.

The low-noise HEMT devices are fabricated on 2-in $\langle 100 \rangle$ epitaxial wafers using standard UV contact photolithography.

The gate metal is evaporated at an angle such that the gate is offset towards the source within the recess area, with part of the metal effectively covering the recess side wall. This makes possible the reduction in the actual gate length over the channel without an increase in the series gate resistance, made possible by the large gate cross section.

The modifications to the epitaxial structure, together with the gate definition processing, contribute to the reduction in the noise figure, which is mainly a function of the gate-to-source series resistance and the gate length as expressed in Fukui's equation. The gate length is nominally 0.4 to 0.5 μm and the source-to-drain spacing is 3 μm .

The chip photograph is shown in Fig. 2.

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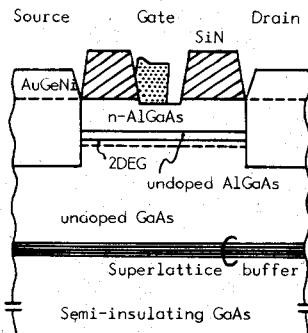


Fig. 1. Cross section of low-noise HEMT.

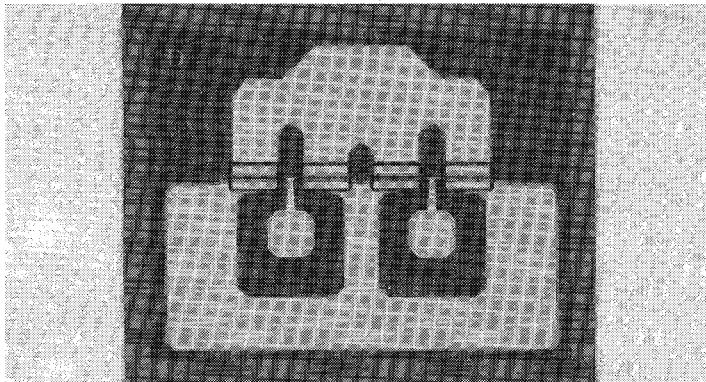


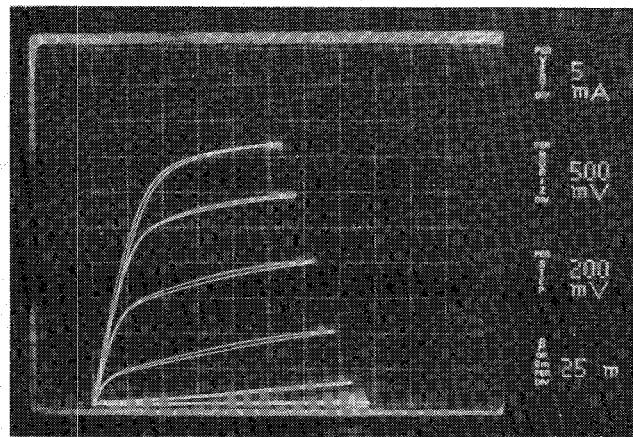
Fig. 2. Chip photograph of low-noise HEMT.

III. DC AND RF PERFORMANCE

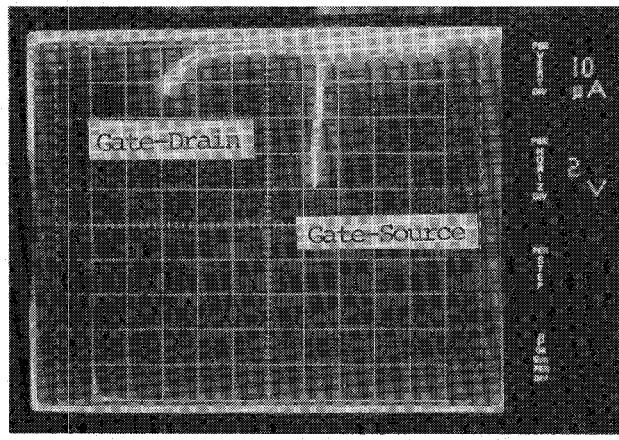
The typical drain current characteristics and the gate Schottky breakdown characteristics of HEMT's having a gate length of $0.5 \mu\text{m}$ and gate width of $200 \mu\text{m}$ are shown in Fig. 3(a) and (b). At 300 K , the maximum extrinsic transconductance was 280 mS/mm at a current density of 120 mA/mm . The intrinsic transconductance calculated from the source resistance was found to have a value of 360 mS/mm . Since the source resistance mainly consists of the 2DEG element between the gate and source together with the ohmic contact resistance, reducing the gate-to-source spacing and decreasing the 2DEG sheet resistance (by increasing the sheet carrier density and mobility) will make possible an even higher extrinsic transconductance than the above value.

The gate breakdown from the Schottky barrier is an important parameter which must be taken into account under actual operating conditions. In general, a lower breakdown voltage of the Schottky gate is observed with HEMT's compared to GaAs MESFET's because of the high donor density in the AlGaAs layer. As shown in Fig. 3(b), typical breakdown voltage values of gate-to-source and gate-to-drain are $> 5 \text{ V}$ and $> 10 \text{ V}$, respectively. An increase of the gate-to-drain breakdown voltage was accomplished by offsetting the gate metal towards the source and optimizing the gate pinchoff voltage, thereby reducing the electric field strength present across the gate and drain. These techniques are comparable to those for GaAs MESFET's.

An analytical model based on Fukui's equation [5], taking the parasitic capacitances of the gate bonding pads



(a)



(b)

Fig. 3. Static characteristics of HEMT. (a) Output characteristics. (b) Schottky reverse characteristics.

into consideration, has been developed as a guide in optimizing the HEMT device performance. The number of gate bonding pads determines the equivalent gate series resistance and the input capacitance, which in turn determines the noise figure and gain.

Various combinations of gate bonding patterns and gate widths were tested for RF performance, as shown in Fig. 4. The total gate capacitance and the series gate resistance can be expressed as follows:

$$C_{gs} = W_g \cdot C_{gu} \cdot L_g + C_{\text{pad}} \cdot n$$

$$R_g = \frac{\text{Rho} \cdot W_g}{12 \cdot t_g \cdot L_g \cdot n^2}$$

where

W_g total gate width,
 C_{gu} capacitance per unit area of gate,
 L_g gate length,
 t_g thickness of gate metal,
 Rho gate metal resistivity,
 C_{pad} capacitance per gate bonding,
 n number of bonds.

The capacitance C_{pad} includes the fringing capacitance of the bonding wires as well as the pad itself. The factor 12

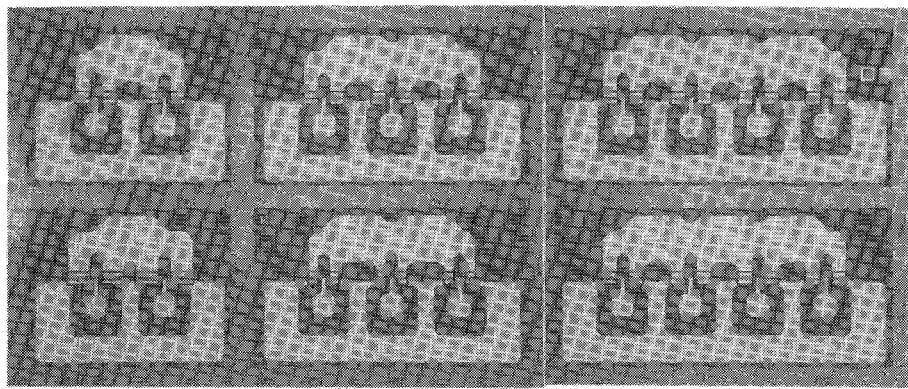


Fig. 4. Photograph of various HEMT test designs.

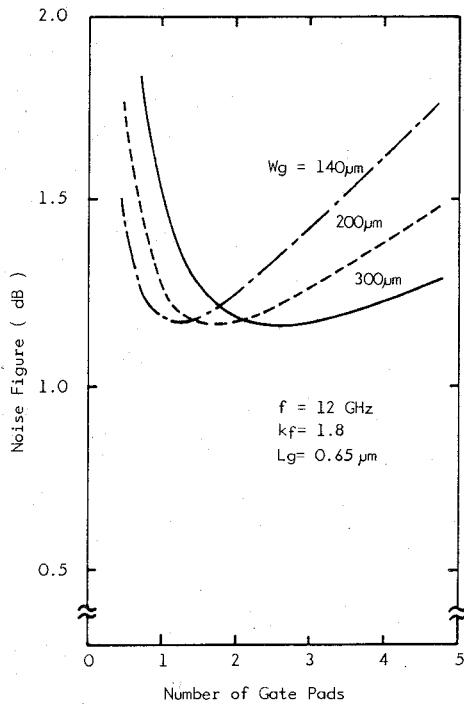


Fig. 5. Calculated noise figure for different gate widths and number of gate pads.

in the R_g equation comes from the distributed nature of current flow along the width of the FET gate.

Using the above formulas for C_{gs} and R_g in Fukui's equation, it was determined that for a device having a 200- μm gate width, two bonding pads give the minimum noise performance, whereas for a 300- μm device either two or three bonding pads will give approximately the same minimum noise figure. The calculated noise figures for 140-, 200-, and 300- μm devices as a function of number of bonds are shown in Fig. 5.

Actual noise figure measurements have confirmed this calculation. It was decided that a 200- μm , two-pad design will be used as the standard device taking into account the impedance requirements, chip area, and other factors.

All noise figure measurements were carried out by mounting the chips on 1.8-mm-square ceramic packages. Noise figures and associated gains were measured at 12 GHz using conventional sleeve tuners. The dependence of

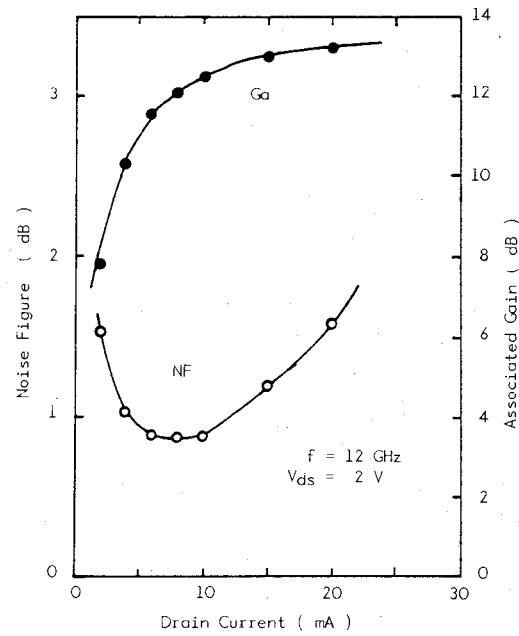


Fig. 6. Noise figure and associated gain as a function of drain current.

noise figure and associated gain on drain current is shown in Fig. 6. Noise figure contours as a function of drain current and drain voltage have been plotted in Fig. 7. The minimum noise figure was 0.83 dB with an associated gain of 12.5 dB at a drain current of 10 mA and drain voltage of 1 V. It can be seen that the HEMT is not sensitive to bias conditions. For 10-mA operation, the device noise figure remains under 1.0 dB from 0.5 to 3 V. With a drain voltage fixed at 1.5 V, the noise figure stays under 1.0 dB from 4 to 18 mA. These minimum noise figure values are comparable to previously reported HEMT's having 0.25- μm gate lengths fabricated by direct-write electron beam (EB) lithography on epitaxial layers grown by MBE [6], [7]. The maximum gain is observed at about 15 mA and 1.6 V. By considering circuit requirements, a bias condition of 10 mA at 2 V has been selected as the standard measurement condition.

The noise figure circles shown on the Smith chart in Fig. 8 show that the HEMT is capable of very broad band operation, having a 50- Ω unmatched noise figure of 1.77 dB. This value is about 1.0 dB better than that of a

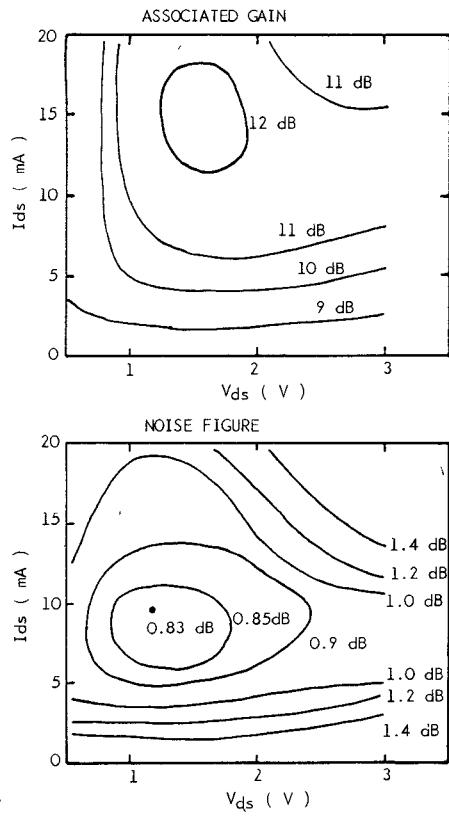


Fig. 7. Map of noise figure and associated gain as a function of drain voltage and current.

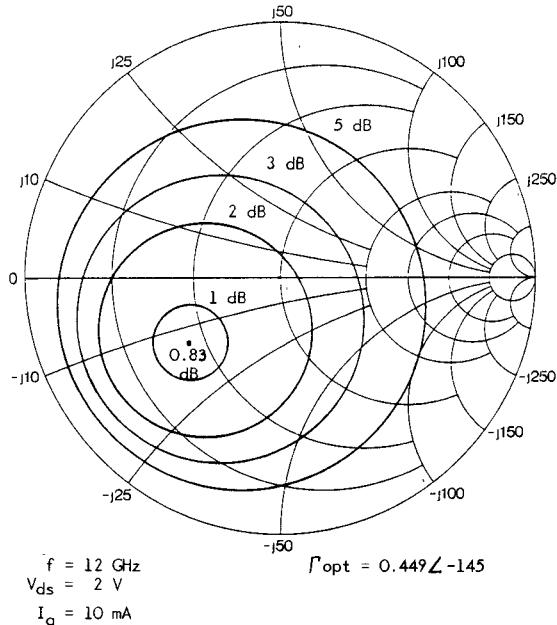


Fig. 8. Noise figure circles of low-noise HEMT.

conventional MESFET. Thus, the HEMT is more tolerant of input mismatching, and is well suited for wide-band MMIC designs. The high transconductance of the HEMT results in an f_{max} of over 70 GHz.

In addition to 12-GHz noise performance measured at room temperature, the devices were thermoelectrically cooled to -20°C to measure the temperature dependence [8].

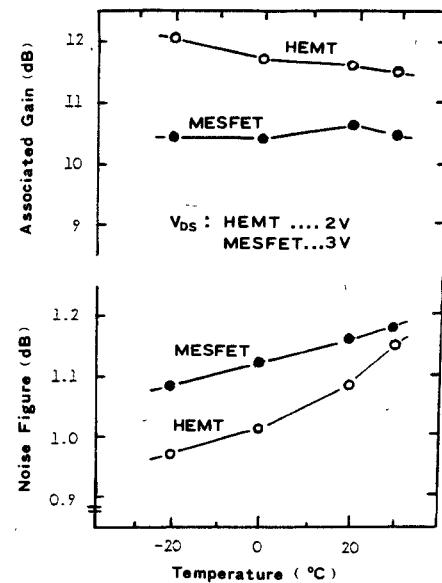


Fig. 9. Temperature dependence of low-noise HEMT.

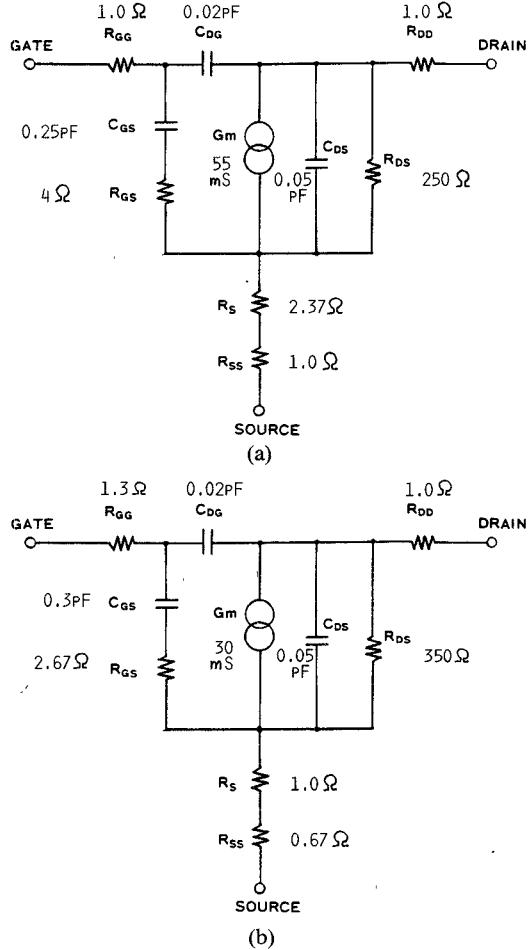


Fig. 10. (a) HEMT equivalent model. (b) MESFET equivalent model.

As shown in Fig. 9, the HEMT's have shown a larger dependence ($0.1\text{dB}/20^{\circ}\text{C}$) than that of the MESFET's ($0.05\text{dB}/20^{\circ}\text{C}$) at a temperature of around 10°C . (The HEMT's used in this experiment were selected for matched performance at room temperature with the MESFET's for comparison purposes.)

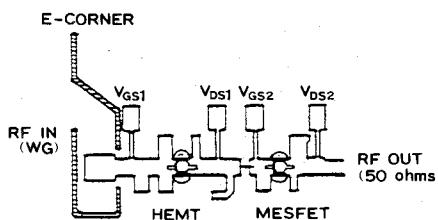


Fig. 11. Circuit pattern of two-stage amplifier using HEMT.

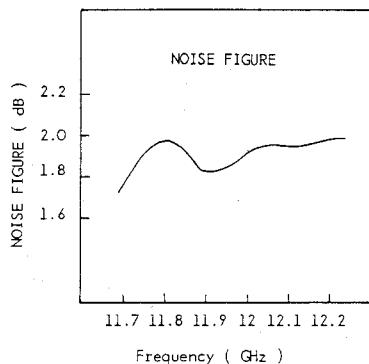


Fig. 12. Noise figure of two-stage amplifier.

The equivalent circuit of the HIFET chip has been determined from S -parameters taken directly from on-wafer measurements using a network analyzer. The reference planes are located on the pad surface. The nominal values of the model elements are shown in Fig. 10(a). A typical model of a 0.5- μm -long, 300- μm -wide GaAs MESFET is shown in Fig. 10(b) for comparison.

A simple two-stage low-noise amplifier for 12-GHz DBS converter systems has been built and tested to evaluate the device performance. The circuit is depicted in Fig. 11. The first stage uses a HEMT device, biased at 10 mA at a drain voltage of 2 V. The second stage uses a conventional MESFET. The input signal entering the waveguide is transferred to the microstrip using an E-corner, and the matching network transforms the 50- Ω impedance to the FET's gamma-optimum. As shown in Fig. 12, the overall noise figure of the two-stage circuit is less than 2.0 dB throughout the 500-MHz bandwidth required for DBS reception in the U.S. and Japan. The microstrip pattern used for this HEMT amplifier is only slightly different from that used for a MESFET amplifier, indicating a high degree of drop-in compatibility with conventional 0.5- μm MESFET devices currently available. The HEMT is very suitable for the first stage of DBS and other satellite receiving systems, where low-noise performance will be required at low cost and in large quantities.

IV. CONCLUSIONS

Low-noise HEMT's fabricated using AlGaAs/GaAs heterointerface structures have been successfully developed by combining standard photolithographic techniques with MOCVD technology. Excellent performance, including a noise figure of 0.83 dB and an associated gain of 12.5 dB at 12 GHz at room temperature, has been demonstrated.

A thin superlattice buffer and a 10- \AA -thick undoped AlGaAs layer were introduced to increase the mobility of 2DEG at the heterointerface. The nominal gate length of 0.5 μm , formed by an angle evaporation lift-off technique, also contributed to an improvement in both RF performance and breakdown voltage.

Further refinements of the HEMT process and device technology directed at the reduction of parasitic elements will allow an even lower noise figure than those reported here.

The feasibility of high-performance HEMT devices for general-purpose microwave applications based on the high-productivity MOCVD process has been demonstrated.

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REFERENCES

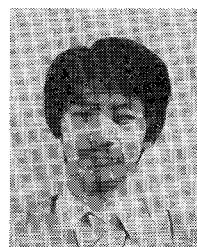
- [1] K. Joshi *et al.*, "Low-noise HEMT with self-aligned gate structure," in *Extended Abstracts of the 16th Conf. on Solid State Devices and Materials*, 1984, pp. 347-350.
- [2] M. Laviron *et al.*, "Ultra low-noise and high frequency operation of TEGFET made by MBE," *Physics*, vol. 129b, pp. 376-379, 1985.
- [3] K. Shibata, B. Abe, H. Kawasaki, S. Hori, and K. Kamei "Broadband HEMT and GaAs FET amplifiers for 18-26.5 GHz," *IEEE MTT-S Digest*, June 1985, pp. 547-550.
- [4] H. Takakuwa, *et al.*, "Low-noise microwave HEMT using MOCVD," *IEEE Trans. Electron Devices*, vol. ED-33, pp. 595-600, May 1986.
- [5] H. Fukui, "Optimal noise figure of microwave GaAs MESFET's," *IEEE Trans. Electron Devices*, vol. ED-26, pp. 1032-1037, July 1979.
- [6] M. Sholley *et al.*, "36.0-40.0 GHz HEMT low-noise amplifier," *IEEE MTT-S Digest*, June 1985, pp. 5455-558.
- [7] U. K. Mishra, S. C. Palmateer, P. C. Chao, P. M. Smith, and J. C. M. Hwang, "Microwave performance of 0.25-micron gate length high electron mobility transistors," *IEEE Electron Device Lett.*, vol. EDL-6, pp. 142-145, Mar. 1985.
- [8] K. Kamei *et al.*, "Low-noise high electron mobility transistor," in *GaAs and Related Compounds Symp.*, 1984, pp. 545-550.



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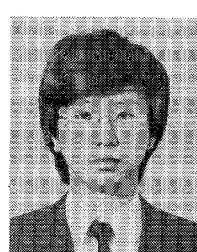
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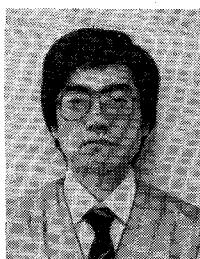


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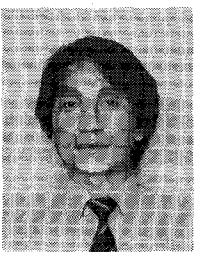


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